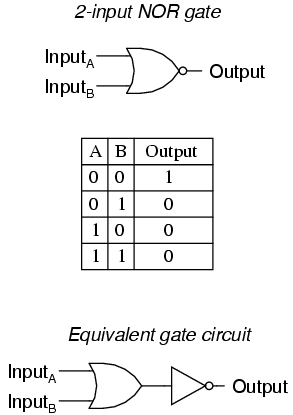
**Circuit Diagram & Truth Table:**



**Code:**

* **Design Module**

module gate(z,x,y);

input x,y;

output z;

assign z=~(x|y);

endmodule

* **TestBench**

module test;

reg a,b;

wire c;

gate x(c,a,b);

initial

begin

a=1'b0; b=1'b0;

#20

a=1'b0; b=1'b1;

#20

a=1'b1; b=1'b0;

#20

a=1'b1; b=1'b1;

#20

$finish;

end

endmodule

**Output:**

